60 GHz Capacitively Probe-Fed Patch Arrays with Suspended Elements

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***Abstract*—A major drawback of current millimeter-wave technologies used for integration of phased arrays on a chip is low efficiency (5-10%) and consequently low realized gain. In this work, we present integrated antenna arrays on silicon that exhibit radiation efficiency of >80% at 60 GHz. This is achieved by suspending the radiating elements of a phased array in air using micro-electro-mechanical systems (MEMS) processes, effectively replacing a lossy silicon substrate (under each element) with air. In the latest design we used capacitive feeding with pin and patch height of 40 and 60 µm, respectively. Finite element simulation results verify the performance of the array. A finite array with 5×5 elements achieved -10-dB bandwidth of 1.7 GHz. Array is well matched at 60 GHz with S_{11}<−19 dB. Maximum realized gain (at broadside) is 20 dBi with sidelobe level of -13.3 dB. The efficiency is calculated to be 89%. Integration of antenna on a chip, provides enormous advantage in miniaturization of the systems and is essential for next-generation active electronically scanned arrays.**

***Index Terms*—Suspended, MEMS, Phased Array, High Efficiency.**

I. INTRODUCTION

Conservative estimates predict that cellular data traffic will grow 40-70% annually in the foreseeable future, implying the need for networks to support greater than 1000 times the current data traffic [1-3]. In recent years there has been great interest in 60 GHz antennas due to large unlicensed bands available at 57-64 GHz [4]. This band is a great candidate for next-generation short-range communication links. However, there are several challenges for successful realization of millimeter-wave communication systems. One such challenge is that the signal propagation at millimeter-wave frequencies is impaired by severe path-loss and shadowing effects [5]. Transmit and receive beamforming networks with many (e.g., ≥100) antennas per terminal are natural approach to countering the increased path loss at 60 GHz band. As a result, next generation antennas operating at this band need to be capable of electronic scanning while exhibiting a high gain.

Currently there are two approaches for on-chip antennas. In the first approach, the antenna is positioned on the substrate resulting in massive radiation losses. This is due to low resistivity of silicon causing most of the field couple to silicon substrate (with dielectric constant of 11.7) instead of radiating in free space. Improvements to efficiency are possible by thinning down the substrate or using high-resistivity substrate which are both undesirable options since they are limited and costly. Despite these improvements, the antenna radiation efficiency is in the order of 5-10% or less [6-8]. The state of the art approach utilizes a ground plane on the substrate with a thin layer of silicon dioxide (SiO_2) (e.g. 5 µm in thickness) separating a radiating elements from the ground layer [9]. Due to close proximity of the transmission line and radiating elements to the ground plane, the conductive losses dominate resulting in antenna radiation efficiency in the order of 45% or less. The key limitation here is finite thickness of SiO_2 layer in a standard Bi-CMOS processes used for fabricating active components such as T/R modules. To avoid cracking in the thick dielectric layer, metal fences (vias) are designed and fabricated within the dielectric layer that contribute to additional losses. Furthermore, higher silicon dioxide thickness (between the ground plane and the antenna elements) increases the fabrication cost of the antenna array.

In contrast to the aforementioned approaches in realizing integrated phased arrays, this paper presents a novel architecture that uses MEMS suspended radiating elements together with capacitively-fed patch to achieve >80% efficiency. This approach has a few unique features. For instance, by suspending the patch, the effective dielectric constant of the substrate is reduced to 1. As a result by reducing conductive, dielectric, and surface wave losses, the efficiency of the antenna is increased. More important, by reducing effective dielectric constant, the array is able to scan much larger volume compared to conventional patch array antennas. We have also improved on our previous work that used aperture coupled micro strip feed network [10]. Unlike our previous design, the pin/capacitor feeding scheme provides better compatibility and easier monolithic integration with a CMOS T/R substrate. This paper is structured as the following. In Section II, basic design and architecture of the phased array is discussed. Fabrication process is presented in Section III. Simulation results – including impedance matching, efficiency, and scanning – are reported in Section IV.

II. PHASED ARRAY ARCHITECTURE

A. Unit Cell Design

Successful implementation of the next-generation antenna array at 60 GHz will depend on a simple – yet

important – factor: Ease of integration of the antenna and the substrate that holds the RF front-end circuits. As mentioned earlier, in a traditional approach, the proximity of the radiating element (patch, dipole, etc.) to a lossy high dielectric constant (silicon) substrate (or the ground plane) is a major source of radiation loss. In cases where the substrate is shielded by a ground plane, a layer of silicon dioxide is used for separation between the radiating element and the ground plane [11]. Given the size of the wave length (λ=5 mm at 60 GHz) and current technology limitations to fabricate thick SiO_2 layer, the maximum possible oxide thickness (5-15 µm) is still well below the required thickness to avoid ohmic losses and achieve high radiation resistance (e.g. $\lambda/10 \approx 500$ µm for a patch array at 60 GHz). To address the aforementioned shortcoming, we propose a novel suspended phased array structure that improves efficiency and scanning performance of the array while maintaining the required bandwidth.

The unit cell schematic of the suspended patch array is shown in Fig.1. As illustrated, the patch is suspended 60 µm above the ground plane with a thick SU-8 posts defined by a photolithography process. These posts occupy a small area, thus, have a minor impact on the radiation pattern of the patch. We have recently characterized the electrical properties of the SU-8 at millimeter wave and terahertz bands [12]. The radiating element can be fabricated on a thin membrane or – as shown in Fig.1 – on a thick dielectric superstrate. Unit cell size is 3 mm × 3 mm. The patch is fed with a 40-µm-height pin forming a capacitive scheme. Each pin is fed directly by a T/R module located underneath elements. The pins are fabricated by metallization of the second set of SU-8 posts.

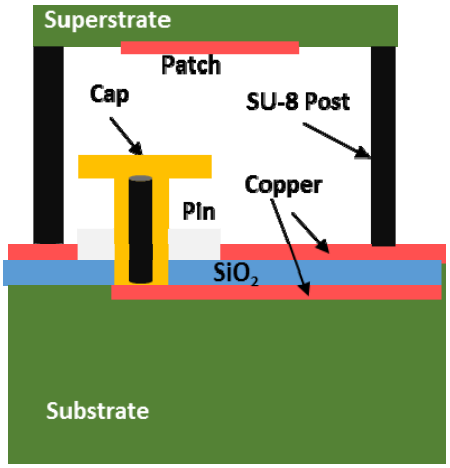

Fig. 1: Schematic cross section of the proposed pin-fed suspended patch array.

B. *Finite Array Design*

Schematic 3D view of the suspended phased array is shown in Fig 2. The array size is chosen to be 5×5 for the ease of simulation, fabrication, and testing. The array size is 15 mm × 15 mm. As mentioned earlier, this architecture is suitable for active electronically scanned arrays. Larger array sizes can also be considered in future to achieve a higher gain. Fabrication and simulation results are reported in the next sections.

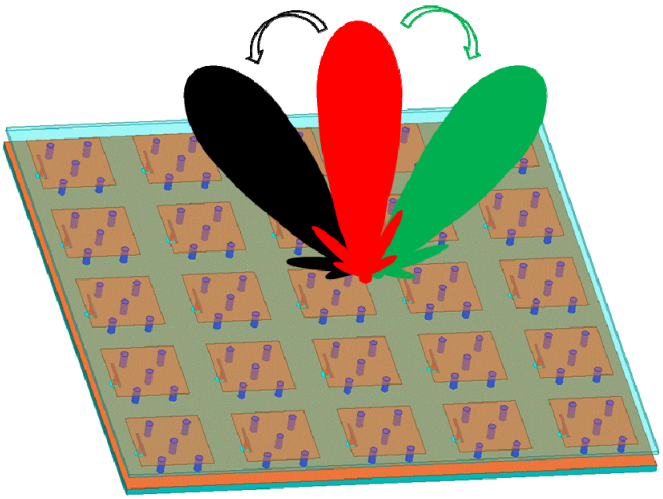

Fig. 2: 3D schematic of high-efficiency phased array with 25 elements. Each patch is suspended on 5 posts and fed by capacitive pin.

III. FABRICATION

The fabrication process of the array is as following. First, the feed lines were fabricated by pattering a 1-µm-thick gold layer on a silicon substrate. A 3-µm-thick SiO_2 layer was then deposited, patterned, and etched to form a pin slot. Next, the ground plane was patterned using a gold layer. Furthermore, 40-µm-thick SU-8 photo resist was spin coted and patterned to form the posts for pins. Then, 1 µm conformal gold layer was deposited and etched to form capacitive caps. On a separate 100-µm-thick quartz substrate, a 1 µm gold layer was deposited and patterned followed by spin coating and patterning a 60 µm thick SU-8 layer to form the posts for suspended patch. Lastly, the two wafers were aligned and bonded together to form the final array structure.

IV. SIMULATION RESULTS

ANSYS HFSS was used for the simulation of the unit cell of an infinite an array. We also used the same tool for the simulation of the finite 5×5 element array. The impedance matching (at broad side) is shown in Fig. 3. The antenna is well matched at 60 GHz with S_{11}<−19 dB. The −10-dB impedance bandwidth is 1.7 GHz. This bandwidth is sufficiently large for most applications. However, we note that the bandwidth is smaller than the array we previously reported in [10] due to reduced ground plane height and capacitive feeding architecture.

As mentioned earlier, successful implementation of millimeter-wave antenna arrays for next-generation high data-rate communication dictates scanning capability. This is especially important for mobile devices. Simulation results for the scanning performance of the finite array in two cardinal planes are shown in Fig 4. Antenna patterns show

maximum realized gain of 20 dBi at broad side. Depending on the application, the gain can easily be increased by designing a larger array. The array is capable of scanning down to 45° in both *E* and *H* planes. Compared to the broadside, the gain is reduced by 4 dB at 45°. The sidelobes are acceptable and are about −13.3 dB level. Total radiation efficiency of the array is calculated to be 89%.

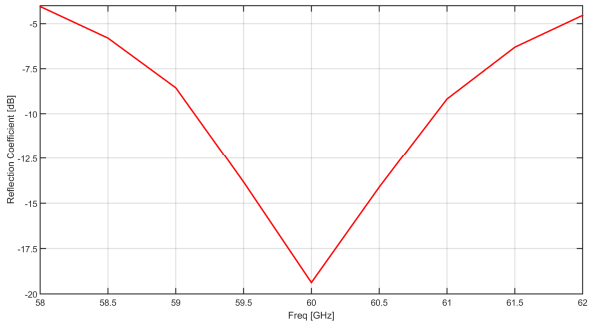

Fig. 3: Simulation results showing reflection coefficient (S_{11}) as a function of frequency. Minimum S_{11} is −19 dB and bandwidth is approx. 1.7 GHz.

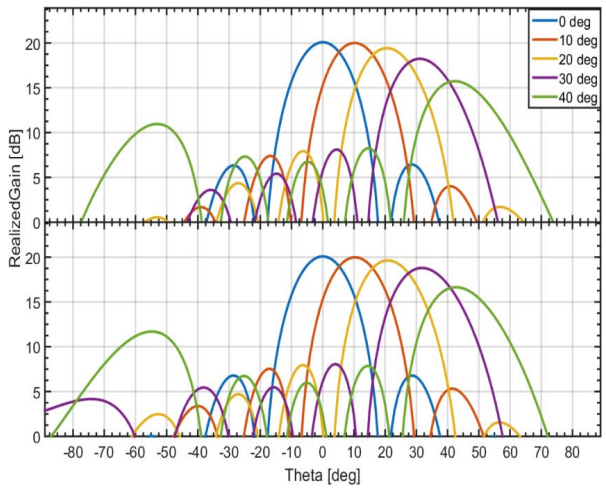

Fig. 4: Simulation results for the antenna pattern showing realized gain as a function of scanning angle for *E*-plane (top) and *H*-plane (bottom).

V. CONCLUSION

In this paper we presented a new design to improve on-chip phased array antenna efficiency and realized gain at 60 GHz. This is achieved by polymer-core capacitively-fed and suspended radiating elements. Achieved gain is 20 dBi with −13.3 dB sidelobes level. The 5×5 (25 elements) array is capable of scanning ± 45° in *E* and *H* planes. In this design, antenna is directly fed from below. The area under the ground plane can be used for front-end electronics. This saves valuable semiconductor space. This antenna will be tested by terminating all but the center element. The latter will be excited by microstrip line and RF probes. Further enhancements to the bandwidth, efficiency, and scanning performance is also possible by reducing grating lobes and terminating the fields at the edge of the array. Design, simulation, fabrication, and measurement results will be presented at the conference.

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